**HDMI test**

Revision history

|  |  |  |  |
| --- | --- | --- | --- |
| Revision | Date | Description | Author |
| 0.1 | 2017-09-13 | Initial | HuiboZhong |
| 0.2 |  |  |  |
|  |  |  |  |

### HDMI 2.0 RX PHY

#### Test Strategy Overview

The　HDMI 2.0 PHY is designed to minimize the effort required to get the finished product chip into production with minimum test time and minimum test development. Software is provided with the IP to create test vectors that utilize the PHY’s Built-In-Self-Test (BIST) capability and JTAG port to test the PHY in production. Test development time is minimized by placing sufficient BIST hardware in the IP to compare analog values with high and low limits in the IP and simply scan out a pass or fail result for easy vector comparison on a digital tester.

#### ATE related PAD

ATE\_TEST\_IN:

|  |  |  |
| --- | --- | --- |
| Pad name | ATE\_Test\_In | Signal name |
| QE0\_0 | ATE\_IN[0] |  |
| QE0\_1 | ATE\_IN[1] | PDDQ |
| QE0\_2 | ATE\_IN[2] | CONT\_EN |
| QE0\_3 | ATE\_IN[3] | BIST\_EN |
| QE0\_4 | ATE\_IN[4] |  |
| QE0\_5 | ATE\_IN[5] |  |
| QE0\_6 | ATE\_IN[6] | SVRET\_MODEZ |
| QE0\_7 | ATE\_IN[7] | CFG\_CLK\_FREQ[０] |
| I2S\_WS2 | ATE\_IN[8] | CFG\_CLK\_FREQ[１] |
| I2S\_SDI2 | ATE\_IN[9] | I2C\_JTAGZ |
| I2S\_SDO2 | ATE\_IN[10] |  |
| I2S\_CLK2 | ATE\_IN[11] |  |
| I2S\_WS3 | ATE\_IN[12] |  |
| I2S\_SDI3 | ATE\_IN[13] | PHY\_RESET |
| I2S\_SDO3 | ATE\_IN[14] |  |
| I2S\_CLK3 | ATE\_IN[15] |  |

HDMI\_PAD

|  |  |
| --- | --- |
| Pad name | Signal name |
| HDMI\_RREF | HDMI\_RREF |
| HDMI\_RXCP | HDMI\_RXCP |
| HDMI\_RXCN | HDMI\_RXCN |
| HDMI\_RX2P | HDMI\_RX2P |
| HDMI\_RX2N | HDMI\_RX2N |
| HDMI\_RX1P | HDMI\_RX1P |
| HDMI\_RX1N | HDMI\_RX1N |
| HDMI\_RX0P | HDMI\_RX0P |
| HDMI\_RX0N | HDMI\_RX0N |

JTAG\_SPI PAD

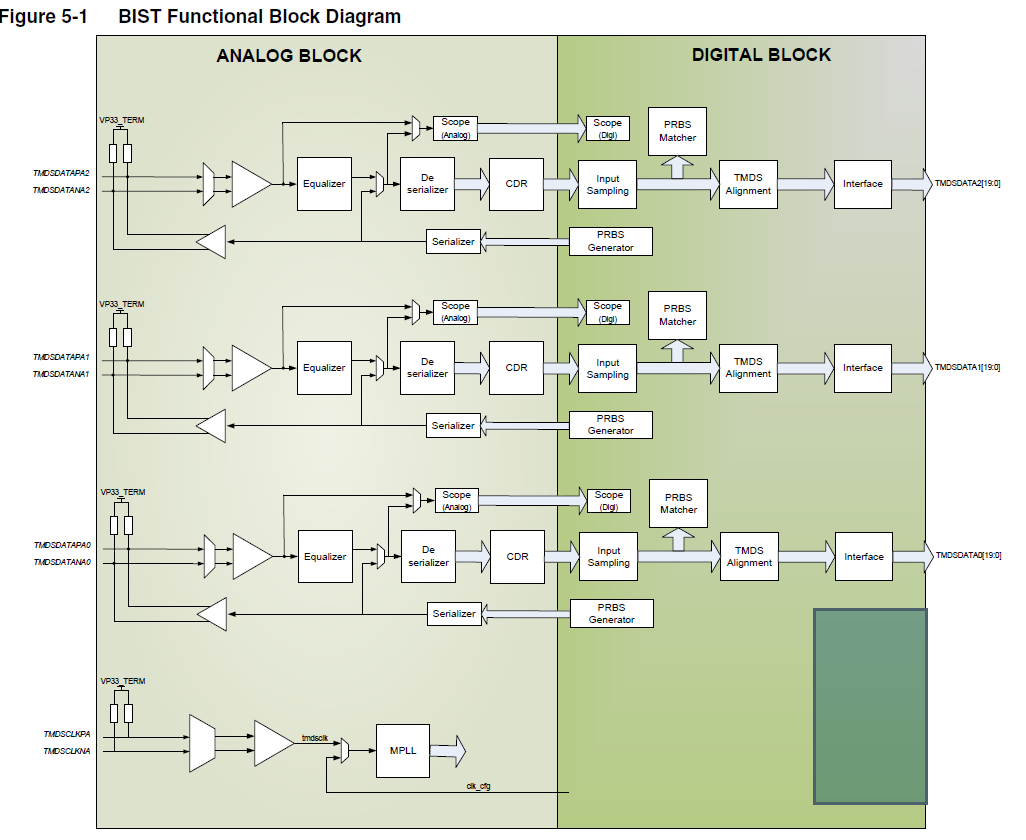
|  |  |
| --- | --- |
| Pad name | Signal name |
| SPI\_MS3\_DI | SPI\_DBG\_DI |
| SPI\_MS3\_DO | SPI\_DBG\_DO |
| SPI\_MS3\_SCLK | SPI\_DBG\_SCLK |
| SPI\_MS3\_CS0N | SPI\_DBG\_CSN |
| SPI\_M2\_DI | TEST\_JTAG\_TDI |
| SPI\_M2\_DO | TEST\_JTAG\_TDO |
| SPI\_M2\_SCLK | TEST\_JTAG\_TCK |
| SPI\_M2\_CS0N | TEST\_JTAG\_TMS |

ATE\_TEST\_OUT

|  |  |  |
| --- | --- | --- |
| Pad name | ATE\_Test\_out | Signal name |
| PCLK1 | ATE\_TEST\_OUT[0] |  |
| DE1 | ATE\_TEST\_OUT[1] | BISTDONE |
| VSYNC1 | ATE\_TEST\_OUT[2] | BISTOK |
| HSYNC1 | ATE\_TEST\_OUT[3] |  |
| QE1\_0 | ATE\_TEST\_OUT[4] |  |
| QE1\_1 | ATE\_TEST\_OUT[5] |  |
| QE1\_2 | ATE\_TEST\_OUT[6] |  |
| QE1\_3 | ATE\_TEST\_OUT[7] |  |
| QE1\_4 | ATE\_TEST\_OUT[8] |  |
| QE1\_5 | ATE\_TEST\_OUT[9] | CONT\_OUT[0] |
| QE1\_6 | ATE\_TEST\_OUT[10] |  |
| QE1\_7 | ATE\_TEST\_OUT[11] | CONT\_OUT[2] |
| PCLK0 | ATE\_TEST\_OUT[12] | CONT\_OUT[3] |
| DE1 | ATE\_TEST\_OUT[13] | CONT\_OUT[4] |
| VSYNC1 | ATE\_TEST\_OUT[14] | CONT\_OUT[5] |
| HSYNC1 | ATE\_TEST\_OUT[15] |  |

#### BIST

The hdmi 2.0 RX PHY implements an internal BIST that enable testing all three channels on port A. During BIST testing, data is generate inside the PRBS module, then sent to the analog front-end (AFE) block, Insidethe AFE, the data is serialized, and based on the selected BIST test (long and sort), the data is injected on the analog receiver path.

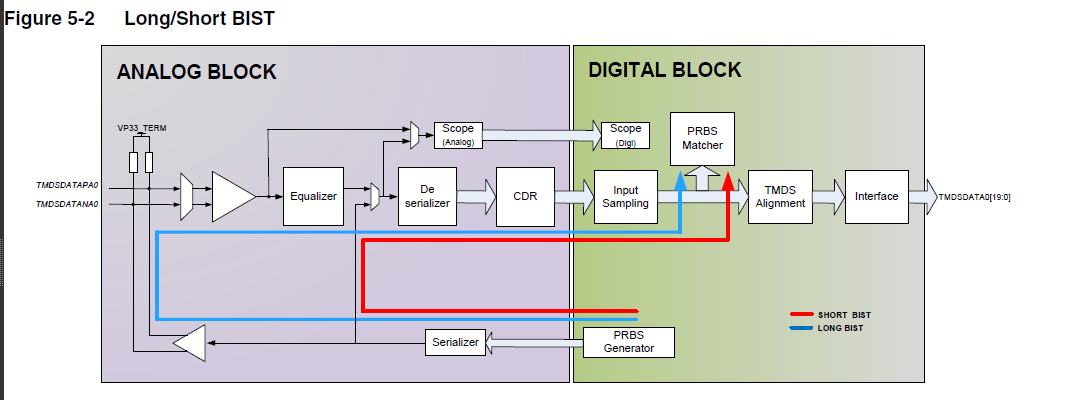


In long-BIST testing, the data is injected on port A, terminations (differential data generated by TX driver); in Short-BIST, the data is injected before the slicers.

During the long BIST, a 50-ohm pull resistor must be connected externally between each data line of PORT A and 3.3V power supply. Those external components must be used only during a long-BIST test. This 50-ohm resistor is applied in the phy internal.

In long-BIST testing, data is injected on port A’s termination, the data then passes through the Receiver block, equalizer (in the test, the equalizer is configured to a flat response), slicers, and finally to the digital blocks. Here, the sampled data is cross-checked with data generated by the PRBS module inside the pattern detector block. If the coming data on the three channels matches the data generated by the PRBS modules, the bist\_ok bit in register ox0C or the BIST ok pin is asserted.

In short-BIST testing, data is injected before the slicers, then passed through slicer to the digital block,. Here the sampled data is cross-checked with the data generated by the PRBS module inside the Pattern Detector block. If the coming data on the three channels matches the data generated by the PRBS modules, the bist\_ok bit in register ox0C or the BIST ok pin is asserted.



BIST requires a clock that is by default, the internal CFGCLK (system clock).

Alternatively, you can apply an external clock through the TMDSCLKPA/TMDSCLKNA signal provide the clock signal meets the HDMI specification requirements.

In both cases, the clock frequency must be 25-100MHz. you can use this configuration to test the clock lane.

BIST TEST Setup:

CFGCLK = 50Mhz (soc provided)

Internal data = 3.4Gbps

BIST mode: short bist

1. Supply
2. Inject CFGCLK
3. Perform a PHY reset
4. Set PDDQ to 1’b1
5. Set PHY\_RESET to 1’b1
6. Configure the PHY clock

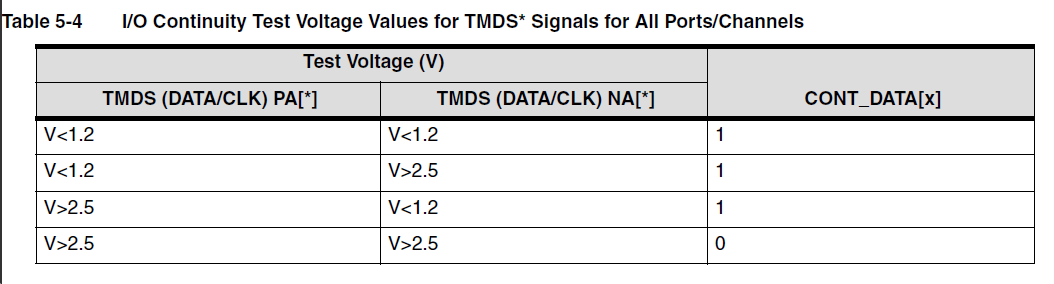
a. Set PHY\_RESET to 1’b0

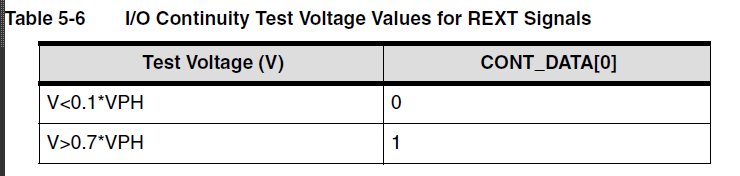
b. Set CFGCLK\_FREQ [1:0] to 2’b10 (default value)

1. MPLL configuration
2. Configure BIST by writing to the JTAG interface.
3. Start BIST test by setting PDDQ to 1’b0
4. When BIST test completes, check for errors by reading from JTAG interface
5. Perform a reset
6. Set PDDQ to 1’b1
7. Set PHY\_RESET to 1’b1

#### I/O continuity Test

The test drives a digital signal from external ATE circuitry or IC –level pins to a PHY analog I/O (TMDSDATAP/NA [2:0], TMDSCLKP/NA, REXT) and captures the signal via a digital bus. The digital bus must be connected to an external, latching circuitry, which should be implemented at the SOC level. To enable this test to be performed, the PHY must be placed in Power-down mode, and the test’s control enable signal (CONT\_EN) must be asserted. In the case, the PHY disables all circuitry not required for the test and turns on only the path required to pass the digital input signal arriveing at the I/O pads to a digital cell, which the routes the signal to aa digital buss (CONT\_DATA[5:2] , CONT\_DATA[0] to be captured by the external latching circuitry . The CONT\_DATA [5:2], CONT\_DATA [0] outputs are only valid when CONT\_EN is enabled





CONT\_DATA[0] REFRES\_S and REFRES\_F (HDMI\_REXT in Sirius)

CONT\_DATA[2] TMDSCLKPA/TMDSCLKNA pins (HDMI\_RXCP/HDMI\_RXCN)

CONT\_DATA[3] TMDSDATAPA2/TMDSDATANA2 pins (HDMI\_RX2P/HDMI\_RX2N)

CONT\_DATA[4] TMDSDATAPA1/TMDSDATANA1 pins (HDMI\_RX1P/HDMI\_RX1N)

CONT\_DATA[5] TMDSDATAPA0/TMDSDATANA0 pins (HDMI\_RX0P/HDMI\_RX0N)

#### CDR testing

HDMI is a source- synchronous interface, and this test checks the HDMI PHY receivers. Most ATE testing is done in a synchronous environment, and external equipment is required to perform this type of testing. This requirement usually involves access to a type of relay matrix to multiplex the external signal to all the channels. This setup takes time to implement and requires a device to be tested on a tester which equipment. The HDMI 2.0 Rx PHY hs a internal PRBS checker and enables the reception of an external clock to provide an alternate jittered clock as the reference clock source . This feature enables the received clock to stress the receiver and CDR, providing more robust testing on the receiver’s CDR. Access to pins TMDSCLKPA/TMDSCLKNAis required.

Test setup:

1. Supply the HDMI PHY

2. Inject a stable clock on the CFGCLK pin. In Sirius, CFGCLK is fix 50MHz

3. Perform a PHY reset.

4. Configure the PHY clock

5. MPLL configuration

6. Configure BIST by writing to JTAG interface

7. Operation for data rates at 3.4Gbps(BIST)

8. Start clock signal injection on the TMDS clock line. (50MHz)

9. Start BIST test by setting PDDQ to 1’b0

10. When BIST test completes, check for errors by reading from the JTAG interface

11. Perform a reset